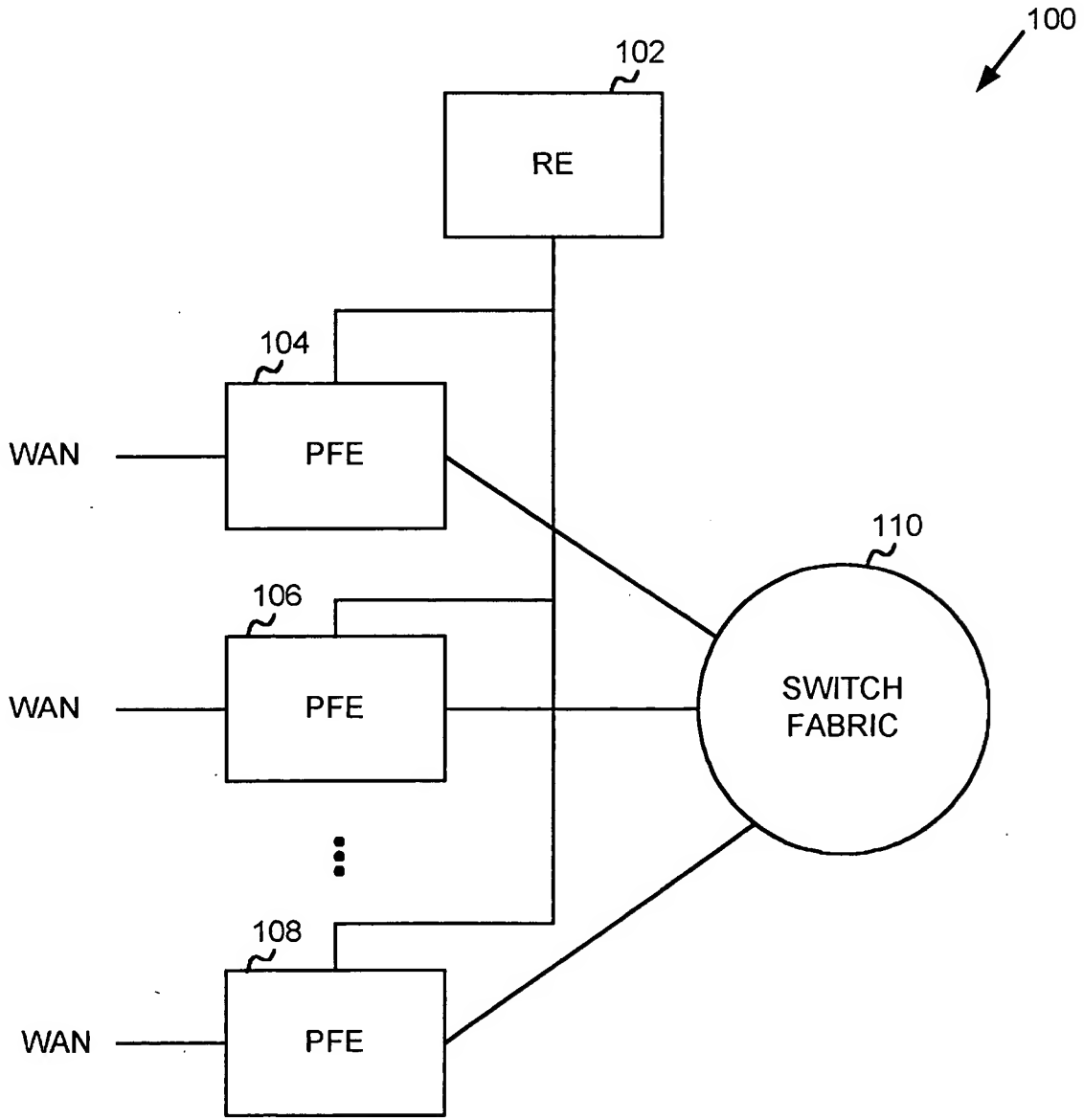

100
102
RE
104
WAN
PFE
106
WAN
PFE
110
SWITCH
FABRIC
108
WAN
PFE

Fig. 1

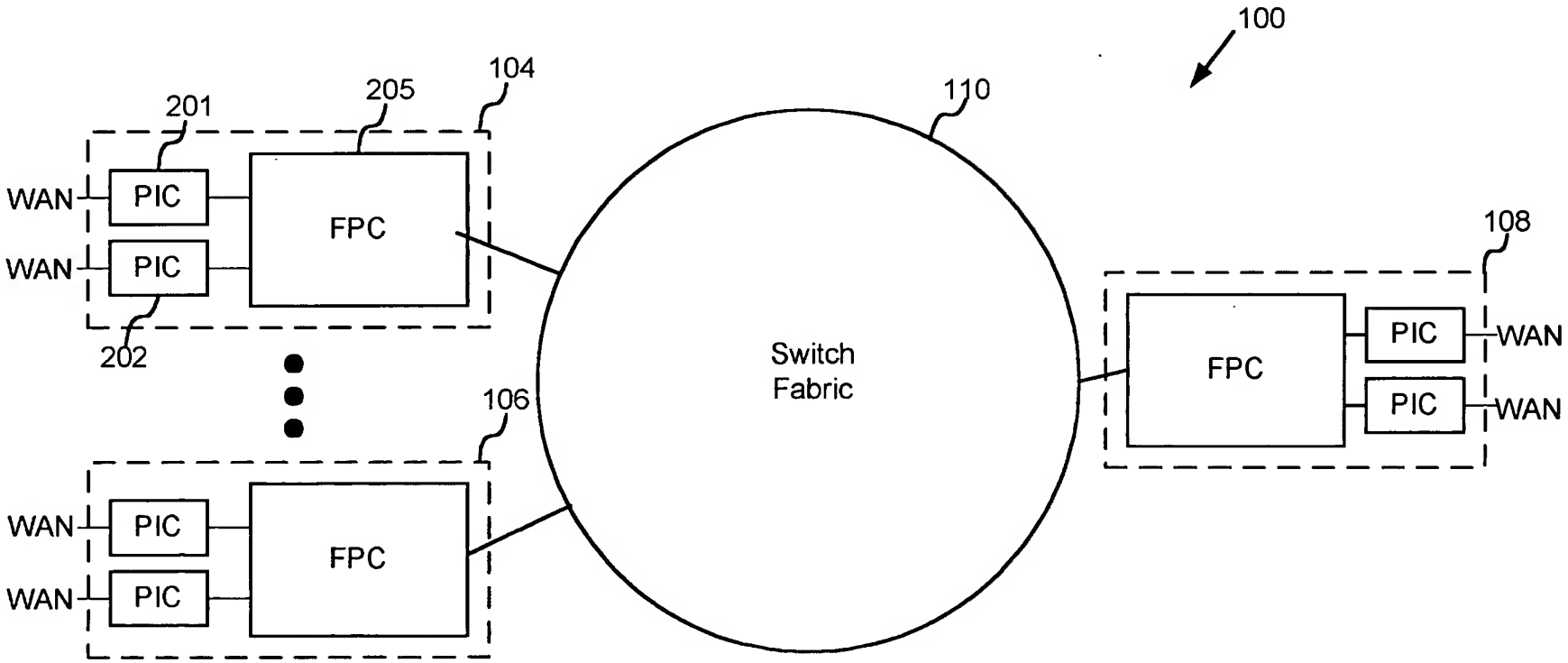
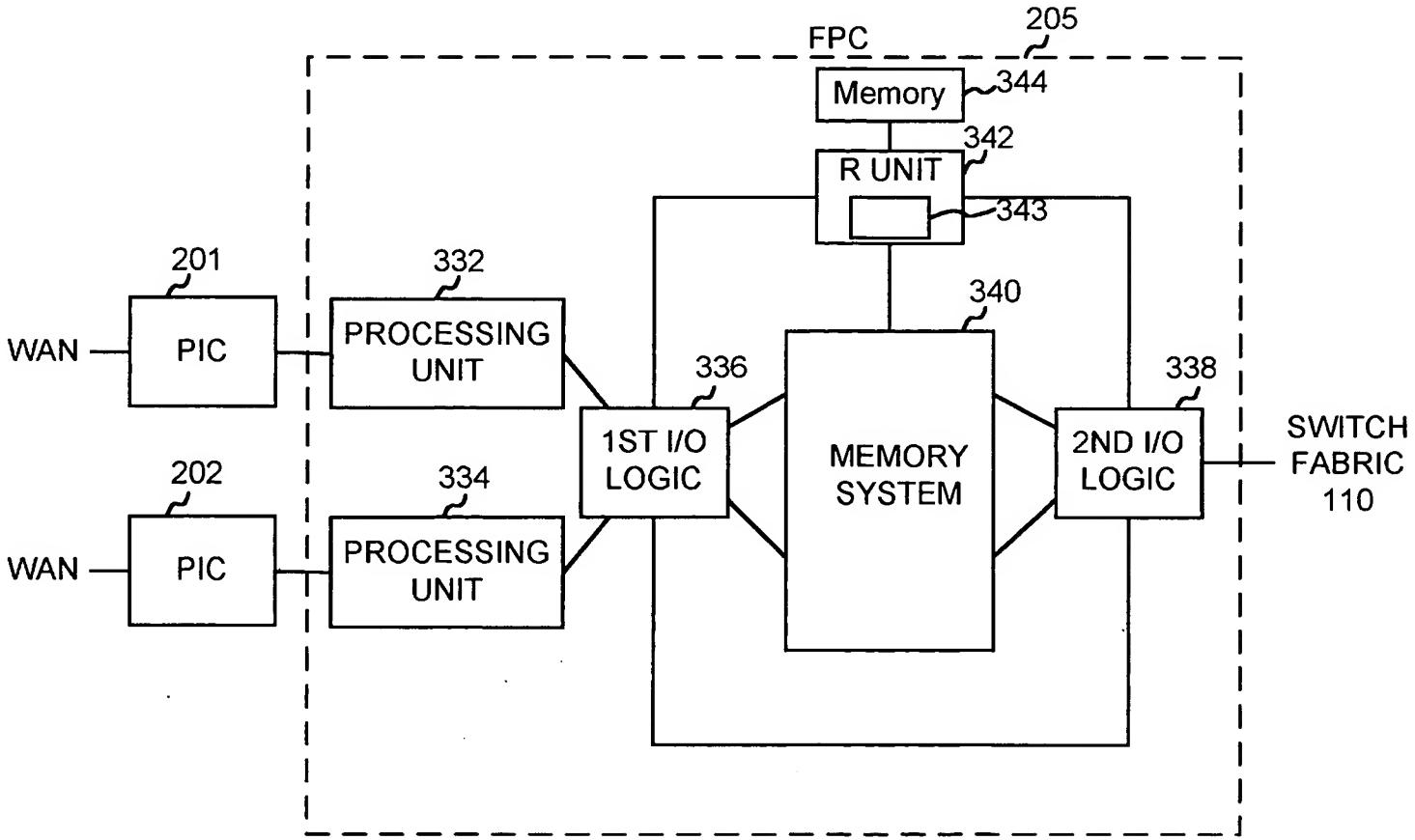

100
104
205
201
110
108
WAN
PIC
WAN
PIC
FPC
202
Switch
Fabric
106
FPC
PIC
WAN
PIC
WAN
WAN
PIC
WAN
PIC
FPC

Fig. 2

Fig. 3


FPC
205
Memory
344
R UNIT
342
343
201
332
340
WAN
PIC
PROCESSING UNIT
336
338
1ST I/O LOGIC
MEMORY SYSTEM
2ND I/O LOGIC
SWITCH FABRIC 110
202
334
WAN
PIC
PROCESSING UNIT

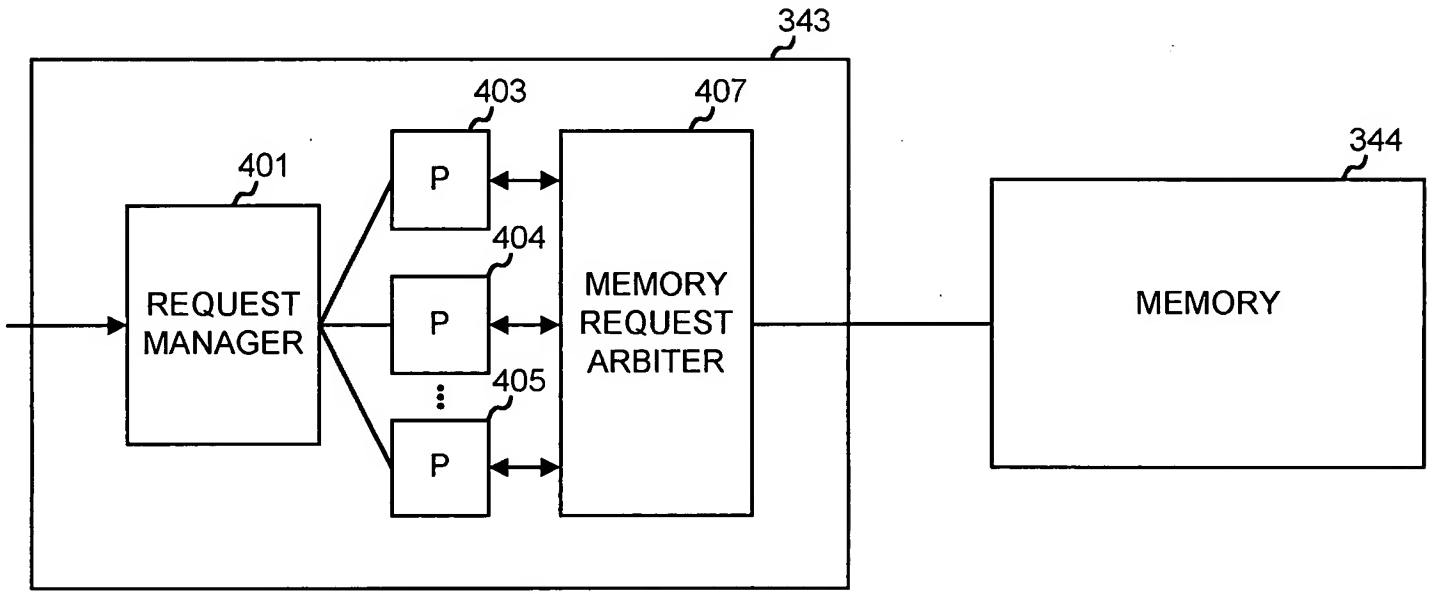

343
403
407
401
344
P
404
REQUEST
MANAGER
P
MEMORY
REQUEST
ARBITER
MEMORY
405
P

Fig. 4

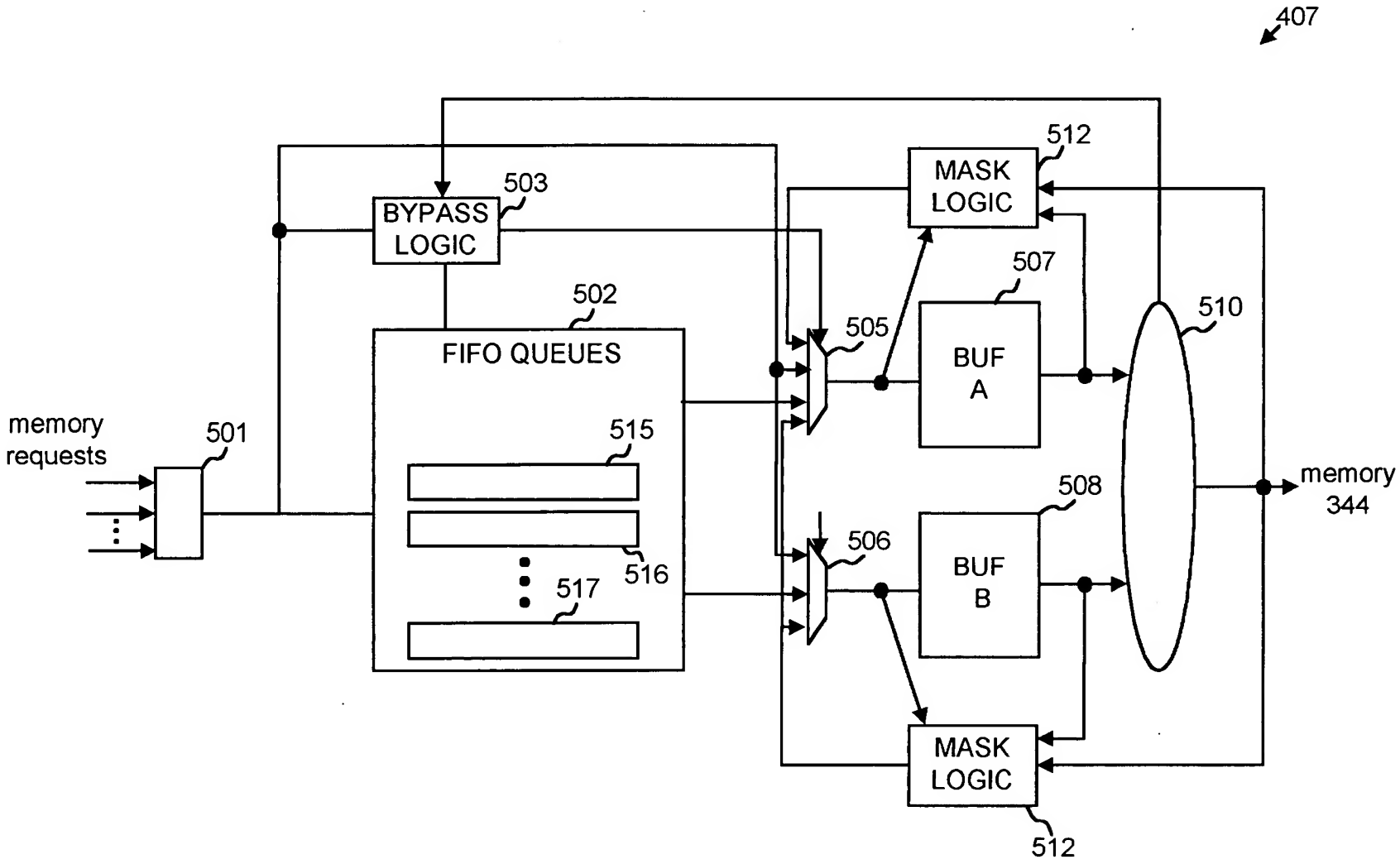

407
512
MASK LOGIC
503
BYPASS LOGIC
507
502
505
510
FIFO QUEUES
BUF A
memory requests
501
515
memory 344
508
506
516
BUF B
517
MASK LOGIC
512

Fig. 5

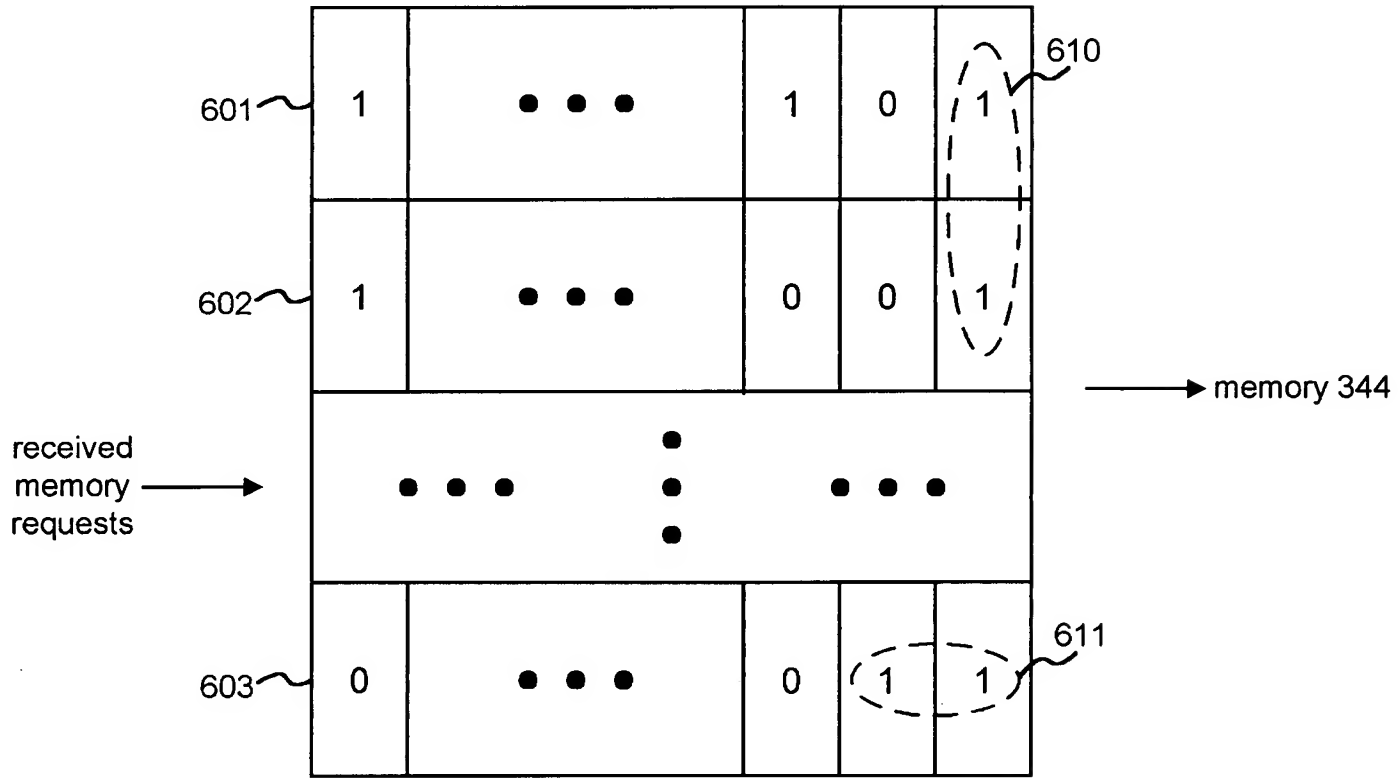

601
602
603
1
1
0
1
0
1
1
0
0
1
0
0
1
1
610
611
received
memory
requests
memory 344

Fig. 6

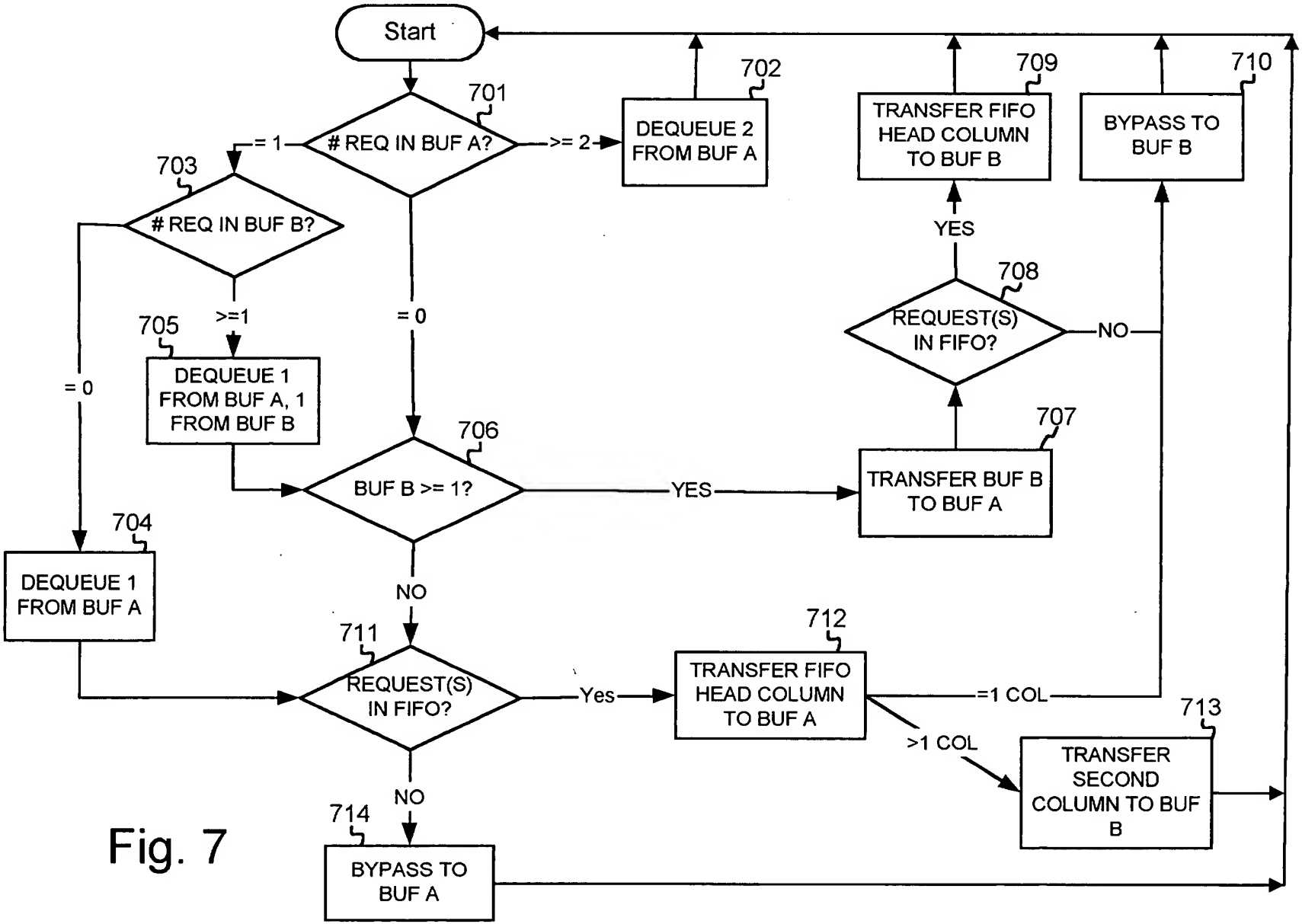

Start
701
REQ IN BUF A?
= 1
>= 2
702
DEQUEUE 2 FROM BUF A
703
REQ IN BUF B?
>=1
= 0
705
DEQUEUE 1 FROM BUF A, 1 FROM BUF B
706
BUF B >= 1?
YES
707
TRANSFER BUF B TO BUF A
708
REQUEST(S) IN FIFO?
NO
YES
709
TRANSFER FIFO HEAD COLUMN TO BUF B
710
BYPASS TO BUF B
= 0
704
DEQUEUE 1 FROM BUF A
NO
711
REQUEST(S) IN FIFO?
Yes
712
TRANSFER FIFO HEAD COLUMN TO BUF A
=1 COL
>1 COL
713
TRANSFER SECOND COLUMN TO BUF B
NO
714
BYPASS TO BUF A

Fig. 7

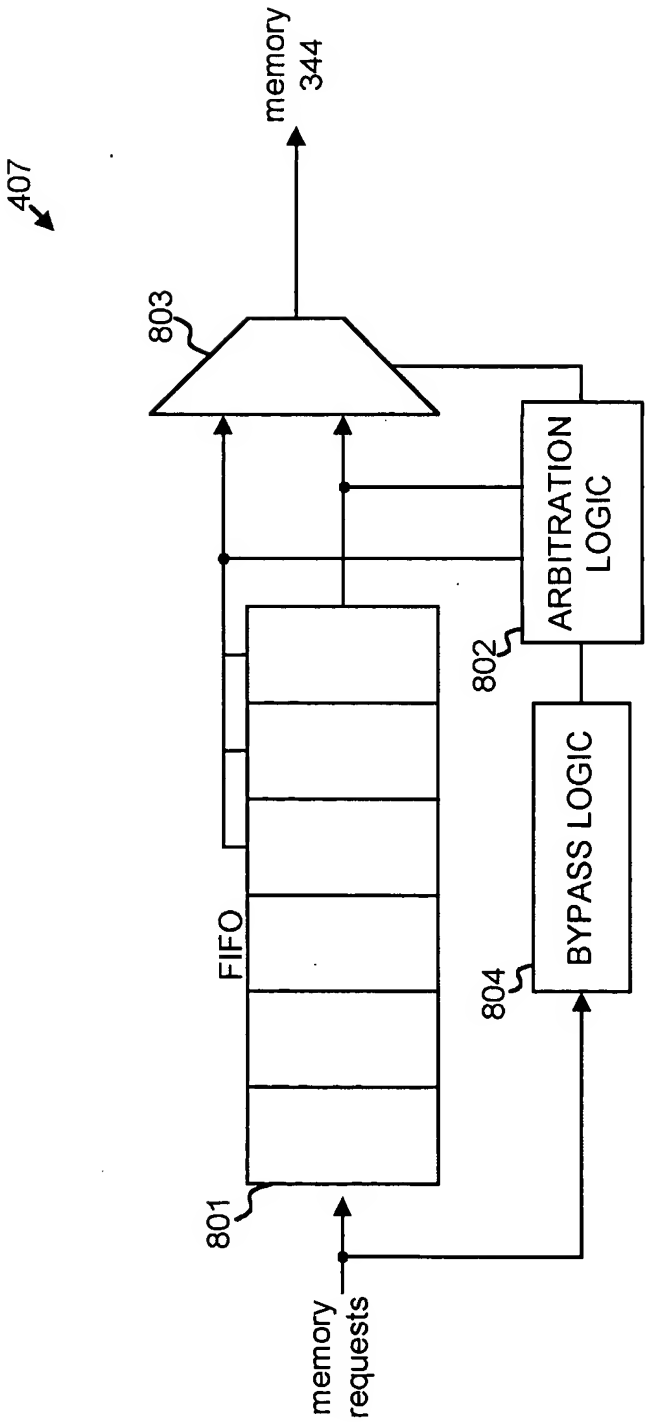

407
memory
344
803
ARBITRATION
LOGIC
802
FIFO
BYPASS LOGIC
804
801
memory
requests

Fig. 8